



I, Tadahiko Itoh, a Patent Attorney of Tokyo, Japan having my office at 32nd Floor, Yebisu Garden Place Tower, 20-3 Ebisu 4-Chome, Shibuya-Ku, Tokyo 150-6032, Japan do solemnly and sincerely declare that I am the translator of the attached English language translation and certify that the attached English language translation is a correct, true and faithful translation of Japanese Patent Application No. 2003-088139 to the best of my knowledge and belief.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Tadahiko ITOH
Patent Attorney
ITOH International Patent Office
32nd Floor,
Yebisu Garden Place Tower,
20-3 Ebisu 4-Chome, Shibuya-Ku,
Tokyo 150-6032, Japan



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Date of Application:	March 27, 2003
Application Number:	No. 2003-088139
[ST.10/C]:	[JP2003-088139]
Applicant(s):	FUJITSU LIMITED

December 1, 2003

Commissioner,
Patent Office

Yasuo Imai (Seal)

Certificate No. 2003-3099152

日 本 国 特 許 庁
JAPAN PATENT OFFICE

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出 願 年 月 日 2 0 0 3 年 3 月 2 7 日
Date of Application:

出 願 番 号 特 願 2 0 0 3 - 0 8 8 1 3 9
Application Number:

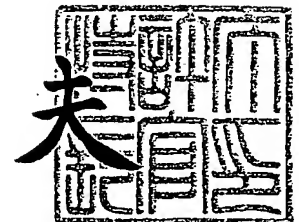
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願 人 富 士 通 株 式 会 社
Applicant(s):

2 0 0 3 年 1 2 月 1 日

特許庁長官
Commissioner,
Japan Patent Office

今 井 康 夫



(Document Name)	Application For Patent
(Reference Number)	0241579
(Date of Submission)	March 27, 2003
(Destination)	Commissioner of Patent Office
	Mr. Shinichiro Oota
(IPC)	H01L 21/90
(Title of the Invention)	SEMICONDUCTOR DEVICE
(Number of Claims)	10
(Inventor)	
(Residence or Address)	c/o FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, Japan
(Name)	Shigetoshi Wakayama
(Inventor)	
(Residence or Address)	c/o FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, Japan
(Name)	Mutsuaki Kai
(Inventor)	
(Residence or Address)	c/o FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, Japan
(Name)	Hiroyuki Kato
(Inventor)	
(Residence or Address)	c/o FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, Japan
(Name)	Masato Suga
(Applicant for Patent)	
(Identification Number)	000005223
(Name)	FUJITSU LIMITED
(Attorney)	
(Identification Number)	100070150
(Residence or Address)	32nd Floor, Yebisu Garden Place Tower 20-3, Ebisu 4-chome, Shibuya-ku, Tokyo, Japan
(Patent Attorney)	
(Name)	Tadahiko Itoh
(Telephone Number)	03-5424-2511

(Indication of Official Fees)

(Prepayment Ledger Number) 002989

(Amount Paid) ¥21,000

(Lists of Submitted Documents)

(Document Name) Specification 1

(Document Name) Drawing 1

(Document Name) Abstract 1

(Number of General Power of Attorney) 0114942

(Proof Requested or Not) Requested

[Name of the Document] Specification

[Title of the Invention]

SEMICONDUCTOR DEVICE

[Claims]

[Claim 1]

A semiconductor device, comprising:
a substrate; and
a multilayer interconnection structure formed on
said substrate,

said multilayer interconnection structure
comprising:

a first guard ring extending continuously in said
multilayer interconnection structure along a periphery of
said substrate; and

a second guard ring extending continuously in said
multilayer interconnection structure along said periphery so
as to be encircled by said first guard ring, said second guard
ring encircling an interconnection pattern inside said
multilayer interconnection structure;

said first and second guard rings being connected
with each other mechanically and continuously by a bridging
conductor pattern extending continuously in a band form along
a region including said first and second guard rings, when
viewed in the direction perpendicular to said substrate.

[Claim 2]

The semiconductor device as claimed in Claim 1,
wherein said bridging conductor pattern is provided at plural
different positions having different heights as measured from
a surface of said substrate.

[Claim 3]

The semiconductor device as claimed in Claims 1 or 2, wherein said bridging conductor pattern is formed in one or more interlayer insulation films in said multilayer interconnection structure.

[Claim 4]

The semiconductor device as claimed in any one of the preceding Claims, wherein said bridging conductor pattern is provided in all of said interlayer insulation films in said multilayer interconnection structure.

[Claim 5]

The semiconductor device as claimed in any one of the preceding Claims, wherein said multilayer interconnection structure has a layered structure in which a plurality of interlayer insulation films each including an interconnection layer corresponding thereto are stacked, and wherein an interconnection layer formed in one interlayer insulation film of said plural interlayer insulation films is connected to an underlying interconnection layer by a via-plug, each of said first and second guard rings having a layered structure identical to that of said multilayer interconnection structure, said bridging conductor pattern being formed at a height identical to that of the interconnection layer in said interlayer insulation film in which said bridging conductor pattern is formed.

[Claim 6]

A semiconductor device, comprising:
a substrate;
a first multilayer interconnection structure
formed on said substrate;
a second multilayer interconnection structure

formed on said first multilayer interconnection structure,
said first multilayer interconnection structure comprising: a first guard ring extending continuously in said first multilayer interconnection structure along a periphery of said substrate; and a second guard ring extending continuously in said first multilayer interconnection structure inside along said periphery so as to be encircled by said first guard ring, said second guard ring encircling an interconnection pattern inside said first multilayer interconnection structure,

said second multilayer interconnection structure comprising: a bridging conductor pattern extending in said second multilayer interconnection structure over a band form region continuously, said bridging conductor pattern mechanically connecting said first and second guard rings with each other; and a third guard ring formed on said bridging conductor pattern.

[Claim 7]

The semiconductor device as claimed in Claim 6, wherein said first and second guard rings are connected mechanically with each other by a first conductor pattern extending continuously along the band form region including said first and second guard rings when viewed in a direction perpendicularly to said substrate with a substantially constant height.

[Claim 8]

The semiconductor device as claimed in Claims 6 or 7, wherein said first multilayer interconnection structure includes an interconnection pattern formed according to a first design rule and the second multilayer interconnection structure includes an interconnection pattern formed by a less

stringent second design rule.

[Claim 9]

The semiconductor device as claimed in any one of the Claims 6 to 8, wherein each of said first and second guard rings is formed of stacking of conductor walls extending along said periphery and having a minimum pattern width prescribed by said first design rule, said first and second guard rings being formed with a minimum interval prescribed by said first design rule.

[Claim 10]

The semiconductor device as claimed in any one of the Claims 7 to 9, wherein said first multilayer interconnection structure has a layered structure in which a plurality of interlayer insulation films each including an interconnection layer corresponding thereto and having a first specific dielectric constant, are stacked, and wherein an interconnection layer formed in an interlayer insulation film of said plurality of interlayer insulation films is connected to an interconnection layer formed in an underlying interlayer insulation film by a via-plug, each of said first and second guard rings having a layered structure identical to that of said first multilayer interconnection structure, said second multilayer interconnection structure having a layered structure in which a plurality of interlayer insulation films each including an interconnection layer corresponding thereto and having a second specific dielectric constant are stacked and an interconnection layer formed in an interlayer insulation film of said plurality of interlayer insulation films is connected to an interconnection layer formed in an underlying interlayer insulation film by a via-plug, said third guard ring having a layered structure

identical to that of said second multilayer interconnection structure, said bridging conductor pattern being formed at a height identical to the height of said interconnection layer in said interlayer insulation film in which said bridging conductor pattern is formed,

said first specific dielectric constant being smaller than said second specific dielectric constant.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention generally relates to semiconductor devices and more particularly to a semiconductor device having a multilayer interconnection structure.

[0002]

Conventionally, increase of operational speed has been attempted in semiconductor devices by way of device miniaturization according to the scaling law. On the other hand, in recent semiconductor integrated circuits of high integration density, it is insufficient to use a single interconnection layer for wiring semiconductor devices of enormous numbers formed on the substrate, and thus, a multilayer interconnection structure in which a number of interconnection layers are stacked with intervening insulation films is used generally for providing the necessary interconnection.

[0003]

In the semiconductor integrated circuit having such a multilayer interconnection structure, on the other hand, it is practiced to provide an anti-moisture guard ring

along a periphery of a chip so as to block penetration of moisture or gas. Such a guard ring extends in the multilayer interconnection structure continuously along the periphery of the chip and interrupts the penetration path of moisture or gas, which may be formed at the interface between an interlayer insulation film and an interconnection layer.

[0004]

[Prior Art]

FIGS.1(A) and 1(B) show the construction of a semiconductor integrated circuit 10 having such a conventional guard ring, wherein FIG.1(A) is a cross-sectional view of the foregoing semiconductor integrated circuit 10 including a guard ring 1, while FIG.1(B) is a plane view showing the entirety of the chip of the semiconductor integrated circuit 10.

[0005]

Referring to FIG.1(A), the semiconductor integrated circuit 10 is formed on a device region 11A defined on a Si substrate 11 by a device isolation structure 11B and includes active devices such as a MOS transistor formed on the device region 11A.

[0006]

The semiconductor integrated circuit 10 includes a first multilayer interconnection structure 12 formed on the substrate and includes therein interconnection layers L1 - L4 and via-plugs P1 - P6 and a second multilayer interconnection structure 13 formed on the first multilayer interconnection structure 12, wherein the second multilayer interconnection structure 13 includes therein interconnection layers L5 - L7 and via-plugs P7 and P8. In

FIG.1, it should be noted that illustration of the interlayer insulation films in the multilayer interconnection structures 12 and 13 is omitted.

[0007]

Further, as shown in the plan view of FIG.1(B), a guard ring 14 is formed on the substrate 11 continuously along the periphery of the chip.

[0008]

Referring to FIG.1(A) again, the guard ring 14 is formed by stacking conductor patterns C1 - C7 extending continuously along the periphery of the chip respectively in correspondence to the interconnection layers L1 - L7 and conductor walls W1 - W7 also extending continuously along the periphery of the chip respectively in correspondence to plugs Pla and Plb and also the plugs P2 - P7.

[0009]

Such a guard ring 14 has a layered structure corresponding to the multilayer interconnection structures 12 and 13 and thus can be formed at the time of formation of the multilayer interconnection structure by a common process.

[0010]

[Patent Document 1]

Japanese Laid-Open Patent Application No.2-123753(KOUHOU)

[0011]

[Problems to be Solved by the Invention]

In recent ultrafine semiconductor integrated circuits, low dielectric constant films called low-K film having a low specific dielectric constant is used as the

interlayer insulation film for suppressing the problem of parasitic capacitance of wiring. It should be noted that parasitic capacitance of wiring becomes conspicuous with the progress of device miniaturization and becomes a serious problem in high-density integrated circuits. Such a low dielectric constant film includes those films having a specific dielectric constant of 2.0 - 3.0 or less, such as an aromatic hydrocarbon polymer film marketed under the trademark of SiLK or Flare, or a porous film thereof. Such a low dielectric constant film is used predominantly for the lower multilayer interconnection structure 12 located near the substrate 11, in which interconnection patterns are formed with minimum separation.

[0012]

Such a low dielectric constant film generally has the feature of low density in correspondence to the feature of low specific dielectric constant, and because of this, various investigations and proposals have been made for a multilayer interconnection structure that uses a low dielectric constant interlayer insulation film in relation to securing adhesion between the interconnection pattern and the interlayer insulation film.

[0013]

The similar situation applies also to the case of the guard ring 14, and thus, there can be a case in which gap is formed between any of the conductor patterns C1 - C7 such as the conductor pattern C3 and the conductor wall formed adjacent thereto.

[0014]

When a gap is formed in the guard ring, such a part

can serve for the path of moisture or external gas into the multilayer interconnection structure. As shown in FIG.1, moisture or gas thus invaded can cause various problems such as defective contact, increase of resistance, disconnection of interconnection pattern, and the like, when it has caused diffusion into the multilayer interconnection structures 12 and 13. Further, in the case the moisture or gas thus invaded has reached the active device such as a MOS transistor formed on the surface of the substrate 11, there is a possibility that the active device may experience degradation.

[0015]

In order to solve such problems, it has been practiced to provide a guard ring of double structure by using guard rings 14A and 14B as shown in FIG.2, wherein those parts of FIG.2 explained previously are designated by the same reference numerals and the description thereof will be omitted. In the illustrated example, the guard rings 14A and 14B have the same construction as the guard ring 14 of FIG.1.

[0016]

By using such a guard ring of double structure, the probability of invasion of moisture or gas into the multilayer interconnection structures 12 and 13 is reduced significantly.

[0017]

In the construction of FIG.2, however, the moisture or the gas invaded inside the guard ring 14A can cause diffusion in the stacked structure between the guard rings 14A and 14B in the case there is formed a defect somewhere in the outer guard ring 14A extending continuously along the chip periphery and in the case there is formed a defect

somewhere in the inner guard ring 14B extending continuously along the chip periphery as shown in FIG.2. Ultimately, the moisture or gas can enter the region inside the guard ring 14B.

[0018]

Thus, there are cases in which the semiconductor integrated circuit having the guard ring of the double structure of FIG.2 cannot satisfy the reliability and lifetime specified for the semiconductor integrated circuit.

[0019]

Further, in the case of the semiconductor integrated circuit having the guard ring of the double structure of FIG.2, the guard ring occupies substantial area of the substrate 11, and because of this, there arises the problem in that the area for forming the active device or the multilayer interconnection structure is decreased.

[0020]

As explained previously, very minute interconnection patterns having the via-diameter of $0.9\mu\text{m}$ or less, for example, are formed with close separation and thus with high density in the lower multilayer interconnection structure 12, by using a low dielectric interlayer insulation film. On the other hand, in the upper multilayer interconnection structure 13, the design rule for the interconnection pattern is less stringent, and thus, there are cases in which a via-diameter of about $1.7\mu\text{m}$ is used.

[0021]

In such a structure, the separation between the guard rings 14A and 14B is determined substantially by the

via-diameter in the multilayer interconnection structure 13, and there appears a waste region in the multilayer interconnection structure 12 between the guard rings 14A and 14B in which formation of a functional element of the semiconductor device is not possible.

[0022]

Further, it should be noted that an interlayer insulation film of low dielectric constant is generally a low density film as explained previously, and because of this, the low dielectric film generally shows poor mechanical performance such as poor Young modulus. Because of this, there is a tendency in the guard ring 14 of FIG.1 that concentration of stress occurs in the conductor patterns C1 - C4 or in the conductor walls W1 - W5 corresponding to the lower multilayer interconnection structure 12 when an external stress is applied. Thereby, the conductor patterns C1 - C4 or the conductor walls W1 - W5 may easily undergo deformation. When deformation is caused in any of the conductor patterns C1-C4 or in the conductor walls W1 - W5, there is formed an invasion path of moisture or external gas as explained previously.

[0023]

Accordingly, it is a general object of the present invention to provide a new and useful semiconductor device in order to solve the problems mentioned above.

[0024]

One specific object of the present invention is to provide a semiconductor device having a guard ring capable of surely blocking invasion of moisture or gas into the semiconductor device from outside.

[0025]

Another object of the present invention is to provide a semiconductor device having a guard ring occupying a small area and yet capable of surely blocking invasion of moisture or gas into the semiconductor device.

[0026]

[Means to Solve the Problems]

The present invention eliminates the problems mentioned above by providing a semiconductor device, comprising: a substrate; and a multilayer interconnection structure formed on said substrate, said multilayer interconnection structure comprising a first guard ring extending continuously in said multilayer interconnection structure along a periphery of said substrate; a second guard ring extending continuously in said multilayer interconnection structure along said periphery so as to be encircled by said first guard ring, said second guard ring encircling an interconnection pattern inside said multilayer interconnection structure; said first and second guard rings being connected with each other mechanically and continuously by a bridging conductor pattern extending continuously in a band form along a region including said first and second guard rings, when viewed in the direction perpendicular to said substrate.

[0027]

According to the present invention, the region between the first and second guard rings is compartmented by the bridging conductor pattern extending continuously along the band form region between the first and second guard rings when viewed in the direction perpendicular to the substrate. Thus, even in the case moisture or gas has invaded to such

a region, further penetration of the moisture or gas to the interior of the semiconductor device is blocked by the foregoing bridging conductor pattern. Thereby, the bridging conductor pattern functions as a compartment wall or a bulkhead. Thus, according to the present invention, by using the two guard rings, invasion of moisture or gas is blocked positively while suppressing the increase of area of the substrate surface occupied by the guard ring.

[0028]

The present invention eliminates the problems mentioned above by providing a semiconductor device, comprising: a substrate; a first multilayer interconnection structure formed on said substrate; a second multilayer interconnection structure formed on said first multilayer interconnection structure, said first multilayer interconnection structure comprising: a first guard ring extending continuously in said first multilayer interconnection structure along a periphery of said substrate; and a second guard ring extending continuously in said first multilayer interconnection structure along said periphery so as to be encircled by said first guard ring, said second guard ring encircling an interconnection pattern inside said first multilayer interconnection structure, said second multilayer interconnection structure comprising: a bridging conductor pattern extending in said second multilayer interconnection structure over a band form region continuously, said bridging conductor pattern mechanically connecting said first and second guard rings with each other; and a third guard ring formed on said bridging conductor pattern.

[0029]

According to the present invention, the area of the substrate occupied by the first and second guard rings is minimized by connecting the first and second guard rings formed in the first multilayer interconnection structure to the third guard ring formed in the second multilayer interconnection structure by way of the bridging conductor pattern.

[0030]

In the semiconductor device of the present invention, a very minute interconnection pattern is formed in the first multilayer interconnection structure of the lower layer by using a stringent design rule, and associated with this, the first and second guard rings are formed by a minute pattern with minute pitch or minute interval. Contrary to this, the design rule is less stringent in the second multilayer interconnection structure of the upper layer where a large via-diameter is used. Thereby, the third guard ring is formed by a wide conductor wall having a comparatively large width in correspondence to the via-diameter. In the present invention, the area of the substrate surface occupied by the guard ring is minimized by providing the first and second guard rings right underneath the third guard ring. Of course, the reliability of the guard ring, and thus the reliability of the semiconductor device, can be improved furthermore by forming a different bridging conductor pattern in the first multilayer interconnection structure so as to bridge the first and second guard rings.

[0031]

[Embodiments of the Invention]

[FIRST EMBODIMENT]

FIG.3 shows the construction of a semiconductor

integrated circuit 20 according to a first embodiment of the present invention.

[0032]

Referring to FIG.3, the semiconductor integrated circuit 20 is formed on a Si substrate 21 having a device region 21A defined by a device isolation structure 21B, and a MOS transistor including a gate electrode 22G and diffusion regions 21a and 21b is formed in the device region 21A such that the diffusion regions 21a and 21b are formed in the Si substrate 21 at both lateral sides of the gate electrode 22G. In FIG.3, it should be noted that illustration of the gate insulation film is omitted. Further, similarly to a usual MOS transistor, the gate electrode 22G is provided with a pair of sidewall insulation films of SiO_2 or SiON .

[0033]

The gate electrode 22G is covered by an interlayer insulation film 22 formed on the substrate 21, wherein the interlayer insulation film 22 forms a part of the first multilayer interconnection structure 31 formed on the substrate 21.

[0034]

Thus, on the interlayer insulation film 22, interlayer insulation films 23 - 26 are formed consecutively, and an interconnection pattern 22W and via-plugs 22P₁ and 22P₂ are formed in the interlayer insulation film 22 so as to fill the wiring groove or via-holes formed in the film 22 by way of a dual damascene process, by filling the wiring grooves or via-holes by a conductor layer and by removing the unnecessary conductor layer on the interlayer insulation film 22 by a CMP (chemical mechanical polishing) process. As a

result of the dual damascene process, the interconnection pattern 22W has a principal surface coincident to the surface of the interlayer insulation film 22. Further, in the illustrated example, the via-plugs 22P₁ and 22P₂ make a contact to the diffusion regions 21a and 21b, respectively.

[0035]

A similar interconnection structure is formed in each of the interlayer insulation films 23 - 26. Thus, in the interlayer insulation film 23, there are formed an interconnection layer 23W and a via-plug 23P, while an interconnection layer 24W and a via-plug 24P are formed in the interlayer insulation film 24. Further, an interconnection layer 25W and a via-plug 25P are formed in the interlayer insulation film 25 and a via-plug 26P is formed in the interlayer insulation film 26.

[0036]

Typically, the interlayer insulation films 23 - 26 are formed of an organic polymer film having a specific dielectric constant of less than 3.0, while the interconnection layers 22W - 25W and the via-plugs 22P₁ and 22P₂ and 23P - 26P are formed of Cu. Further, the interconnection layers 22W - 25W and the via-plugs 22P₁ and 22P₂ and 23P - 26P can be formed also by using Al or an Al alloy or other conductors.

[0037]

On the interlayer insulation film 26, there is formed an interconnection layer 27W typically formed of Al or an Al alloy so as to make a contact with the via-plug 26P, wherein the interconnection layer 27W forms a part of another multilayer interconnection structure 32 formed on the

multilayer interconnection structure 31.

[0038]

Thus, the interconnection layer 27W is covered with an interlayer insulation film 27 and a next interconnection layer 28W is formed on the interlayer insulation film 27. The interconnection layer 28W, in turn, is connected to the interlayer insulation film 27 through a via-plug 27P formed in the interconnection layer 27W. Similarly, the interconnection layer 28W is covered with an interlayer insulation film 28 formed on the interlayer insulation film 27, and a next interconnection layer 29W is formed on the interlayer insulation film 28. The interconnection layer 29W is connected to the interconnection layer 28W through a via-plug 28P formed in the interlayer insulation film 28.

[0039]

In a typical example, the interlayer insulation films 27 and 28 are formed of SiOC or SiO₂ while the interconnection layers 27W - 29W are formed of Al or an Al alloy. Further, the via-plugs 27P and 28P are formed by W (tungsten), and the like.

[0040]

Furthermore, a passivation film 29 of SiN, and the like, is formed on the interlayer insulation film 28.

[0041]

In the semiconductor integrated circuit 20 of FIG.3, an outer guard ring 33A and an inner guard ring 33B are formed so as to extend continuously along the periphery of the substrate such that the interconnection layers in the

multilayer interconnection structures 31 and 32 are encircled. Reference should be made to the plan view of FIG.1(B).

[0042]

Referring to FIG.3, the guard ring 33A includes: a conductor wall 22PA formed in the interlayer insulation film 22 simultaneously to the via-plugs 22P₁ and 22P₂ by the same material thereto so as to extend in the interlayer insulation film 22 continuously along a periphery of the substrate 21 without forming a gap with a width substantially the same as the diameter of the via-plugs; and a conductor pattern 22WA formed in the interlayer insulation film 22 simultaneously to the interconnection layer 22W by the same material thereto so as to extend on the conductor wall 22PA continuously along the periphery of the substrate without forming a gap. Further, in the interlayer insulation film 23, there are formed, as a part of the guard ring 33A, a conductor wall 23PA extending on the conductor pattern 22WA continuously along the periphery of the substrate 21 without forming a gap with a width substantially the same as the diameter of the via-plug 23P, and a conductor pattern 23WA extending on the conductor wall 23PA along the substrate periphery continuously without forming a gap, wherein the conductor wall 23PA is formed simultaneously to the via-plug 23P by the same material, while the conductor pattern 23WA is formed in the interlayer insulation film 23 simultaneously to the interconnection layer 23W by the same material.

[0043]

Further, the guard ring 33A includes: a conductor wall 24PA formed in the interlayer insulation film 24 simultaneously to the via-plug 24P by the same material thereto so as to extend on the conductor pattern 23WA continuously

along the periphery of the substrate 21 with substantially the same width as the diameter of the via-plug 24P without forming a gap; a conductor pattern 24WA formed in the interlayer insulation film 24 simultaneously to the interconnection layer 24W by the same material so as to extend on the conductor wall 24PA continuously along the substrate periphery without forming a gap; a conductor pattern 25WA formed in the interlayer insulation film 25 simultaneously to the interconnection layer 25W by the same material thereto so as to extend on the conductor wall 24PA continuously along the periphery of the substrate without forming a gap; and a conductor wall 25PA formed in the interlayer insulation film 25 simultaneously to the via-plug 25P by the same material thereto so as to extend on the conductor pattern 24WA with a width the substantially the same width as the via-diameter of the via-plug 25P continuously along the periphery of the substrate 21 without forming a gap.

[0044]

In the interlayer insulation film 25, there is formed a conductor pattern 25WA formed simultaneously to the interconnection layer 25W by the same material such that the conductor pattern 25WA extends on the conductor wall 25PA continuously without forming a gap.

[0045]

Further, the guard ring 33A includes a conductor wall 26PA formed simultaneously to the via-plug 26P by the same material thereto so as to extend continuously in the interlayer insulation film 26 on the conductor pattern 25WA with substantially the same width as the diameter of the via-plug 26P along the periphery of the substrate 21 without forming a gap. The guard ring 33A further includes, on the

conductor wall 26PA, a conductor pattern 27WA formed in the interlayer insulation film 27 simultaneously to the interconnection layer 27W by the same material thereto so as to extend on the conductor wall 26PA along the substrate periphery continuously without forming a gap, and a conductor wall 27PA formed simultaneously to the via-plug 27P by the same material thereto so as to extend on the conductor pattern 27WA along the periphery of the substrate circumference continuously without forming a gap.

[0046]

Further, the guard ring 33A includes: a conductor pattern 28WA formed on the conductor wall 27PA in the interlayer insulation film 27 simultaneously to the interconnection layer 28W by the same material thereto so as to extend on the conductor wall 26PA continuously along the periphery of the substrate without forming a gap; and a conductor wall 28PA formed simultaneously to the via-plug 28P by the same material thereto so as to extend on the above-mentioned conductor pattern 28WA continuously along the periphery of the substrate without forming a gap. Further, in the passivation film 29, there is formed a conductor pattern 29WA on the conductor wall 28PA simultaneously to the interconnection layer 29W by the same material as a part of the guard ring 33A.

[0047]

Similarly, the guard ring 33B includes: a conductor wall 22PB formed in the interlayer insulation film 22 simultaneously to the conductor wall 22PA by the same material thereto so as to extend in the interlayer insulation film 22 continuously along the periphery of the substrate 21 with a width substantially the same as the via-diameter of

the via-plug 22P₁ or 22P₂ without forming a gap; and a conductor pattern 22WB formed in the interlayer insulation film 22 simultaneously to the conductor pattern 22WA by the same material thereto so as to extend on the conductor wall 22PB continuously along the periphery of the substrate without forming a gap. Further, in the above-mentioned interlayer insulation film 23, there are provided, as a part of the guard ring 33B, a conductor wall 23PB formed simultaneously to the conductor wall 23PA by the same material thereto so as to extend on the conductor pattern 22WB continuously along the periphery of the substrate 21 with a width substantially the same as the diameter of the via-plug 23P without forming a gap, and a conductor pattern 23WB formed in the interlayer insulation film 23 simultaneously to the conductor pattern 23WA by the same material so as to extend on the conductor wall 23PB along the periphery of the substrate continuously without forming a gap.

[0048]

Further, the guard ring 33B includes: a conductor wall 24PB formed in the interlayer insulation film 24 simultaneously to the conductor wall 24PA by the same material thereto so as to extend on the conductor pattern 23WB along the periphery of the substrate 21 continuously with a width substantially the same as the diameter of the via-plug 24P without forming a gap; and a conductor pattern 24WB formed in the interlayer insulation film 24 simultaneously to the conductor pattern 24WA by the same material thereto so as to extend on the conductor wall 24PB top along the periphery of the substrate continuously without forming a gap. Further, the guard ring 33B includes a conductor pattern 25WB formed in the interlayer insulation film 25 simultaneously to the conductor pattern 25WA with the same material thereto so as

to extend on the conductor wall 24PB continuously along the periphery of the substrate without forming a gap, and a conductor wall 25PB formed in the interlayer insulation film 25 simultaneously to the conductor wall 25PA by the same material thereto so as to extend on the conductor pattern 24WB along the periphery of the substrate 21 with a width substantially the same as the diameter of the via-plug 25P continuously without forming a gap.

[0049]

In the interlayer insulation film 25, there further extends a conductor pattern 25WB formed simultaneously to the conductor pattern 25WA by the same material thereto on the conductor wall 25PB continuously without forming a gap.

[0050]

Further, the guard ring 33B includes a conductor wall 26PB formed simultaneously to the conductor wall 26PA by the same material thereto in the interlayer insulation film 26 so as to extend on the conductor pattern 25WB along the periphery of the substrate 21 continuously a width the same as the diameter of the via-plug 26P without forming a gap. Further, the guard ring 33B includes a conductor pattern 27WB formed on the conductor wall 26PB in the interlayer insulation film 27 simultaneously to the conductor pattern 27WA by the same material thereto so as to extend on the conductor wall 26PB along the periphery of the substrate continuously without forming a gap, and a conductor pattern 27PB formed simultaneously to the conductor wall 27PA by the same material thereto so as to extend on the conductor pattern 27WB continuously along the periphery of the substrate without forming a gap.

[0051]

Furthermore, the guard ring 33B includes: a conductor pattern 28WB formed on the conductor wall 26PB in the interlayer insulation film 27 simultaneously to the conductor pattern 28WA by the same material thereto so as to extend on the conductor wall 27PB continuously along the periphery of the substrate without forming a gap; and a conductor wall 28PB formed simultaneously to the conductor wall 28PA by the same material thereto so as to extend on the conductor pattern 28WB along the periphery of the substrate continuously without forming a gap. Further, in the passivation film 29, there is formed a conductor pattern 29WB on the conductor wall 28PB as a part of the guard ring 33B, simultaneously to the interconnection layer 29W by the same material thereto.

[0052]

Thereby, as can be seen in FIG.3, the conductor pattern 23WA and the conductor pattern 23WB are connected, and there is formed a conductor pattern 23WC extending continuously along the periphery of the substrate 11 as shown in FIG.4. Similarly, the conductor pattern 27WA and the conductor 27WB are connected, and there is formed a conductor pattern 27WC extending continuously along the periphery of the substrate 11 similarly to FIG.4. Thus, the conductor pattern 23WC and the conductor pattern 27C thus formed bridges across the guard ring 33A and the guard ring 33B.

[0053]

As can be seen in FIG.4, the conductor pattern 23WC extends continuously without forming a gap, and thus, there is formed no opening, and the like. Further, as shown in FIG.4

by a dotted line, the upper and lower conductor walls 23PA and 23PB of the conductor pattern 23WC extend continuously along the periphery of the substrate 21 without forming a gap.

[0054]

In the construction of FIG.3, it should be noted that, even in the case there is formed a defect x in a part of the guard ring 33A and also in the guard ring 33B as shown in FIG.5, moisture or gas invaded from outside is blocked by the bridging conductor pattern 23 C as long as the defect is formed in the region isolated by the bridging conductor pattern 23C and cannot invade further into the region inside the guard ring 33B. In other words, the bridging conductor pattern 23C or 27C of the present embodiment functions as a bulkhead or compartment wall compartmenting the region between guard ring 33A and the guard ring 33B into plural compartments.

[0055]

Further, as shown in FIG.6. the path of the external moisture or gas invading into the region inside the guard ring 33B can be blocked by using the conductor pattern 23C even in the case there exists a defect x in each of the guard rings 33A and 33B as long as the defects are formed in the different regions isolated by the bridging conductor pattern 23C. Thus, the reliability of the semiconductor device can be improved significantly. Contrary to this, in the case the guard ring has the structure of FIG.2, the invasion path cannot be blocked and external moisture or gas can penetrate easily to the interior of the semiconductor integrated circuit.

[0056]

FIGS.7(A) - 7(C) show a part of the process of

forming the guard rings 33A and 33B of FIG.3.

[0057]

Referring to FIG.7(A), the interlayer insulation film 22 is formed with the interconnection layer 22W, and the conductor pattern 22WA and the conductor wall 22PA are formed further in correspondence to the guard ring 33A. Further, the conductor wall 22PB and the conductor pattern 22WB are formed in correspondence to the guard ring 33B. The next interlayer insulation film 23 is then formed on the interlayer insulation film 22. Next, the conductor pattern 23A and the via-plug 23P are formed in the interlayer insulation film 23 respectively for the wiring groove 23G and for the via-hole 23H. Simultaneously to this, a groove 23g for the bridging conductor pattern 23C and the grooves 23a and 23b for the conductor walls 23PA and 23PB are formed in the interlayer insulation film 23 in correspondence to the guard rings 33A and 33B.

[0058]

Next, in the step of FIG.7(B), the surface of the interlayer insulation film 23 of FIG.7(A), including the wiring groove 23G, the via-hole 23H and the grooves 23a, 23b and, 23g, it covered with a barrier metal film such as TaN (not illustrated), and thereafter, the groove 23G, the via-hole 23H and the grooves 23a, 23b, 23g are filled with a conductor layer 23Cu such as Cu or W.

[0059]

Further, in the step of FIG.7(C), unnecessary conductor layer 23Cu on the surface of the interlayer insulation film 23 is removed by a CMP (chemical mechanical polishing) process, and a structure in which the wiring groove 23G and the via-hole 23H are filled with the conductor layer

23W and the via-plug 23P respectively and the grooves 23a, 23b and 23g are filled with the conductor walls 23PA and 23PB and the conductor pattern 23WC respectively, is obtained.

[0060]

By repeating such a process, it becomes possible to form the guard rings 33A and 33B without inviting increase of number of the process steps.

[0061]

In the construction of FIGS.7(A) - 7(C), it should be noted that the conductor walls 22PA - 28PA or the conductor wall 22PB- 28PB are formed in alignment in the direction perpendicular to the substrate 11. However, this is not a necessarily condition, and it is also possible to displace the position thereof within the extent of the conductor patterns 23WA - 29WA as shown in the modification of FIG.8. Further, the conductor walls 22PA - 28PA or the conductor walls 22PB - 28PB can be formed also in a zigzag form inside the extent of the conductor pattern 22WA - 29WA or the conductor pattern 22WB - 29WB, which extend in the band-like form along the substrate periphery when viewed in the direction perpendicular to the principal surface the substrate 11.

[0062]

In the present embodiment, it should be noted that the interlayer insulation films 22 - 28 are not limited to the aromatic hydrocarbon polymer film such as SiLK and FLARE, but it is also possible to use various low dielectric constant films such as an MSQ (methyl silsesquioxane) film or a HOSP (hydrido-organic siloxane polymer) film, or a porous film thereof, for the interlayer insulation films 22 - 28.

[0063]

Further, the interconnection layers 22W - 25W and the via-plugs 22P - 26P, and thus, the conductor patterns 22WA - 25WA and 22WB - 25WB, and further the conductor walls 22PA - 26PA and 22PB - 26PB, are not limited to Cu or W, but it is also possible to use Al or an Al alloy in place thereof.

[SECOND EMBODIMENT]

FIG.9 shows the construction of a semiconductor device 40 according to a second embodiment of the present invention, wherein those parts corresponding to the parts explained previously are designated by the same reference numerals and description thereof will be omitted.

[0064]

Referring to FIG.9, the interval between the guard ring 33A and the guard ring 33B on the substrate 21 is reduced in the present embodiment, and associated with this, there is formed, on the conductor pattern 27WC, a single guard ring 33C in the form of stacking of: a single conductor wall 27PC corresponding to the conductor plug 27P; a single conductor pattern 28WC corresponding to the interconnection layer 28W; a single conductor wall 28PC corresponding to the conductor plug 28P; and a single conductor pattern 29WC corresponding to the interconnection layer 29W.

[0065]

As shown in FIG.9, in the semiconductor device of the construction in which the multilayer interconnection structure 32 including therein an interconnection layer of Al or an Al alloy is provided on a high integration density multilayer interconnection structure 31 that uses a low dielectric constant interlayer insulation film by using an

usual interlayer insulation film of SiOC or SiO_2 , it should be noted that the interval between the guard rings 33A and 33B in the multilayer interconnection structure 31 of high integration density can be reduced by applying a stringent design rule of $0.9\mu\text{m}$ or less thereto.

[0066]

With this, the area of the substrate surface occupied by the guard rings 33A and 33B is decreased in the multilayer interconnection structure 31, and the region usable for formation of the active devices and interconnection patterns is increased. Particularly, because the guard ring is formed along the periphery of the substrate or chip, a small decrease of interval of the guard rings 33A and 33B can provide a substantial effect for increasing the substrate area usable for formation of active elements or interconnection patterns.

[0067]

Meanwhile, in the structure of FIG.9, a more relaxed design rule is used in the multilayer interconnection structure 32 of the upper layer, and because of this, there is no decrease in the diameter of the via-plug 27P or 28P, and hence the width of the conductor wall 27PC or 28PC. Thus, as shown in FIG.9, it becomes possible to form the guard ring 33A and 33B in the multilayer interconnection structure 31 so as to locate right underneath the guard ring 33C formed in the multilayer interconnection structure 32.

[0068]

In such a structure, the guard ring 33C is supported by the guard rings 33A and 33B, and because of this, the stress applied to the guard ring 33C is shared by the guard rings 33A and 33B, and thus, the stress applied to each of

the guard rings 33A and 33B formed in the interlayer insulation films 22 - 26 of low Young modulus is reduced. Associated with this, the occurrence of defects in the guard rings 33A and 33B explained with reference to FIG.5 is suppressed, and the reliability of the semiconductor device is improved.

[0069]

FIG.10 shows an example in which the interval between the guard ring 33A and the guard ring 33B is reduced in the semiconductor device 40 of FIG.9 such that the interval between the conductor wall 22PA and the conductor wall 22PB is narrowed to the degree corresponding to the via-diameter.

[0070]

Referring to FIG.10, it should be noted that the guard ring is formed so as to bridge the conductor pattern in each the interlayer insulation films 22 - 25 in this case, and thus, the bridging conductor pattern 22WC bridges the conductor walls 22PA and 22PB in the interlayer insulation film 22. Similarly, the bridging conductor pattern 23WC bridges the conductor walls 23PA and 23PB in the interlayer insulation film 23, the bridging conductor pattern 24WC bridges the conductor walls 24PA and 24PB in the insulation film 24, and the bridging conductor pattern 25WC bridges the conductor walls 25PA and 25PB in the interlayer insulation film 25.

[0071]

According to the construction of FIG.10, the area occupied by the multiple guard ring structure in the high density multilayer interconnection structure formed above the substrate surface and also immediately on the substrate surface is minimized, and it becomes possible to form larger

number of active devices or wiring structures on the substrate.

[0072]

In the present embodiment, too, the interlayer insulation films 22 - 28 is not limited to the aromatic hydrocarbon polymer film such as SiLK or FLARE, similarly to the previous embodiment, and it is possible to use, for the interlayer insulation films 22 - 28, various low dielectric constant films such as an organo-siloxane film including an MSQ (methyl silsesquioxane) film, a HOSP (hydrido-organic siloxane polymer) film, and the like, or a porous film thereof.

[0073]

Further, the interconnection layers 22W - 25W, the via-plugs 22P - 26P, and hence the conductor patterns 22WA - 25WA, 22WB - 25WB, and also the conductor walls 22PA - 26PA and 22PB - 26PB, are not limited to Cu and W, but it is also possible to use Al or an Al alloy in place thereof.

[0074]

(Appendant Note 1)

A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure comprising:

a first guard ring extending continuously in said multilayer interconnection structure along a periphery of said substrate; and

a second guard ring extending continuously in said multilayer interconnection structure along said periphery so as to be encircled by said first guard ring, said second guard

ring encircling an interconnection pattern inside said multilayer interconnection structure;

said first and second guard rings being connected with each other mechanically and continuously by a bridging conductor pattern extending continuously in a band form along a region including said first and second guard rings, when viewed in the direction perpendicular to said substrate.

[0075]

(Appendant Note 2)

The semiconductor device as described in Appendant Note 1, wherein said bridging conductor pattern does not have any of a gap or an opening.

[0076]

(Appendant Note 3)

The semiconductor device as described in Appendant Note 1 or 2, wherein said bridging conductor pattern is provided at plural different positions having different heights as measured from a surface of said substrate.

[0077]

(Appendant Note 4)

The semiconductor device as described as described in any one of the preceding Appendant Notes, wherein said bridging conductor pattern is formed in one or more interlayer insulation films in said multilayer interconnection structure.

[0078]

(Appendant Note 5)

The semiconductor device as described in any one of the preceding Appendant Notes, wherein said bridging

conductor pattern is provided in all of said interlayer insulation films in said multilayer interconnection structure.

[0079]

(Appendant Note 6)

The semiconductor device as described in any one of the preceding Appendant Notes, wherein said multilayer interconnection structure has a layered structure in which a plurality of interlayer insulation films each including an interconnection layer corresponding thereto are stacked, and wherein an interconnection layer formed in one interlayer insulation film of said plural interlayer insulation films is connected to an underlying interconnection layer by a via-plug, each of said first and second guard rings having a layered structure identical to that of said multilayer interconnection structure, said bridging conductor pattern being formed at a height identical to that of the interconnection layer in said interlayer insulation film in which said bridging conductor pattern is formed.

[0080]

(Appendant Note 7)

A semiconductor device, comprising:

a substrate;

a first multilayer interconnection structure formed on said substrate;

a second multilayer interconnection structure formed on said first multilayer interconnection structure,

said first multilayer interconnection structure comprising: a first guard ring extending continuously in said first multilayer interconnection structure along a periphery of said substrate; and a second guard ring extending

continuously in said first multilayer interconnection structure inside along said periphery so as to be encircled by said first guard ring, said second guard ring encircling an interconnection pattern inside said first multilayer interconnection structure,

said second multilayer interconnection structure comprising: a bridging conductor pattern extending in said second multilayer interconnection structure over a band form region continuously, said bridging conductor pattern mechanically connecting said first and second guard rings with each other; and a third guard ring formed on said bridging conductor pattern.

[0081]

(Appendant Note 8)

The semiconductor device as described in Appendant Note 7, wherein said first and second guard rings are connected mechanically with each other by a first conductor pattern extending continuously along the band form region including said first and second guard rings when viewed in a direction perpendicularly to said substrate with a substantially constant height.

[0082]

(Appendant Note 9)

The semiconductor device as described in Appendant Notes 7 or 8, wherein said first multilayer interconnection structure includes an interconnection pattern formed according to a first design rule and the second multilayer interconnection structure includes an interconnection pattern formed by a less stringent second design rule.

[0083]

(Appendant Note 10)

The semiconductor device as described in any one of the Appendant Notes 7 to 9, wherein each of said first and second guard rings is formed of stacking of conductor walls extending along said periphery and having a minimum pattern width prescribed by said first design rule, said first and second guard rings being formed with a minimum interval prescribed by said first design rule.

[0084]

(Appendant Note 11)

The semiconductor device as described in any one of the Appendant Notes 7 to 9, wherein said first multilayer interconnection structure has a layered structure in which a plurality of interlayer insulation films each including an interconnection layer corresponding thereto and having a first specific dielectric constant, are stacked, and wherein an interconnection layer formed in an interlayer insulation film of said plurality of interlayer insulation films is connected to an interconnection layer formed in an underlying interlayer insulation film by a via-plug, each of said first and second guard rings having a layered structure identical to that of said first multilayer interconnection structure,

said second multilayer interconnection structure having a layered structure in which a plurality of interlayer insulation films each including an interconnection layer corresponding thereto and having a second specific dielectric constant are stacked and an interconnection layer formed in an interlayer insulation film of said plurality of interlayer insulation films is connected to an interconnection layer formed in an underlying interlayer insulation film by a via-plug, said third guard ring having a layered structure

identical to that of said second multilayer interconnection structure, said bridging conductor pattern being formed at a height identical to the height of said interconnection layer in said interlayer insulation film in which said bridging conductor pattern is formed,

said first specific dielectric constant being smaller than said second specific dielectric constant.

[0085]

(Appendant Note 12)

The semiconductor device as described in Appendant Note 11, wherein, in said first multilayer interconnection structure, each of said interconnection layers is embedded in a corresponding interlayer insulation film such that a principal surface of said interconnection layer coincides with a principal surface of said corresponding insulation film substantially.

[0086]

(Appendant Note 13)

The semiconductor device as described in any one of the Appendant Notes 7 to 12, wherein said first multilayer interconnection structure uses a film having a specific dielectric constant of less than 3.0 as an interlayer insulation film thereof, and wherein said second multilayer interconnection structure uses a film having a specific dielectric constant of 3.0 or more as an interlayer insulation film thereof.

[0087]

(Appendant Note 14)

The semiconductor device as described in any one of the Appendant Notes 7 to 13, wherein said first multilayer

interconnection structure uses an organic polymer film as an interlayer insulation film thereof.

[0088]

(Appendant Note 15)

The semiconductor device as described in any one of the Appendant Notes 7 to 14, wherein said second multilayer interconnection structure is formed of any of an SiO_2 film or an SiOC film.

[0089]

[Advantages of the Invention]

According to the present invention, the region between the first and second guard rings is compartmented by the bridging conductor pattern extending continuously along the band form region between the first and second guard rings when viewed in the direction perpendicular to the substrate. Thus, even in the case moisture or gas has invaded to such a region, further penetration of the moisture or gas to the interior of the semiconductor device is blocked by the foregoing bridging conductor pattern. Thereby, the bridging conductor pattern functions as a compartment wall or a bulkhead. Thus, according to the present invention, by using the two guard rings, invasion of moisture or gas is blocked positively while suppressing the increase of area of the substrate surface occupied by the guard ring.

[0090]

According to the present invention, the area of the substrate occupied by the first and second guard rings is minimized by connecting the first and second guard rings formed in the first multilayer interconnection structure to the third guard ring formed in the second multilayer

interconnection structure.

[0091]

In the semiconductor device of the present invention, a very minute interconnection pattern is formed in the first multilayer interconnection structure of the lower layer by using a stringent design rule, and associated with this, the first and second guard rings are formed by a minute pattern with minute pitch or minute interval. Contrary to this, the design rule is less stringent in the second multilayer interconnection structure of the upper layer where a large via-diameter is used. Thereby, the third guard ring is formed by a wide conductor wall having a comparatively large width in correspondence to the via-diameter. In the present invention, the area of the substrate surface occupied by the guard ring is minimized by providing the first and second guard rings right underneath the third guard ring. Of course, the reliability of the guard ring, and thus the reliability of the semiconductor device, can be improved furthermore by forming a bridging conductor pattern in the first multilayer interconnection structure so as to bridge the first and second guard rings.

[Brief Description of the Drawings]

[Fig. 1] FIGS.1(A) and 1(B) are diagrams showing the construction of a semiconductor integrated circuit having a conventional multilayer interconnection structure and a guard ring.

[Fig. 2] FIG.2 is a diagram showing the construction of a semiconductor integrated circuit having a dual guard ring structure and further the problems caused in such a semiconductor integrated circuit.

[Fig. 3] FIG.3 is a diagram showing the construction of a

semiconductor integrated circuit according to a first embodiment of the present invention.

[Fig. 4] FIG.4 is a plan view showing a part of FIG.3 with an enlarged scale.

[Fig. 5] FIG.5 is a diagram explaining the function of the guard ring in the semiconductor integrated circuit of FIG.3.

[Fig. 6] FIG.6 is another diagram explaining the function of the guard ring in the semiconductor integrated circuit of FIG.3.

[Fig. 7] FIGS.7(A) - 7(C) are diagrams explaining the fabrication process of the guard ring used in the semiconductor integrated circuit of FIG.3.

[Fig. 8] FIG.8 is a diagram showing a modification of the semiconductor integrated circuit of FIG.3.

[Fig. 9] FIG.9 is a diagram showing the construction of a semiconductor integrated circuit according to a second embodiment of the present invention.

[Fig. 10] FIG.10 is a diagram showing a modification of the semiconductor integrated circuit of FIG.9.

[Description of the Reference Numerals]

10, 20, 40:	Semiconductor Integrated Circuit
11, 21:	Substrate
11A, 21A:	Device Region
11B, 21B:	Device Isolation Structure
12, 13, 31, 32:	Multilayer Interconnection Structure
14, 14A, 14B, 33A, 33B:	Guard Ring
22~26:	Low Dielectric Constant Interlayer Insulation Film
27, 28:	Interlayer Insulation Film
29:	Passivation Film
22W~25W:	Lower Portion Interconnection Layer
27W~29W:	Upper Portion Interconnection Layer
22P1, 22P2, 23P~29P:	Via-Plug

22PA~28PA, 22PB~28PB: Conductor Wall
22WA~29WA, 22WB~29WB: Conductor Pattern
23G: Wiring Groove
23H: Via-Hole
23a, 23b, 23g Groove

[Name of the Document] Abstract

[Abstract]

[Object]

A semiconductor device having a guard ring structure with reliability and occupying a small area is provided.

[Solution Means]

Multiple guard rings are formed and these are bridged by way of bridging conductor pattern extending along a periphery of a chip at plural height positions.

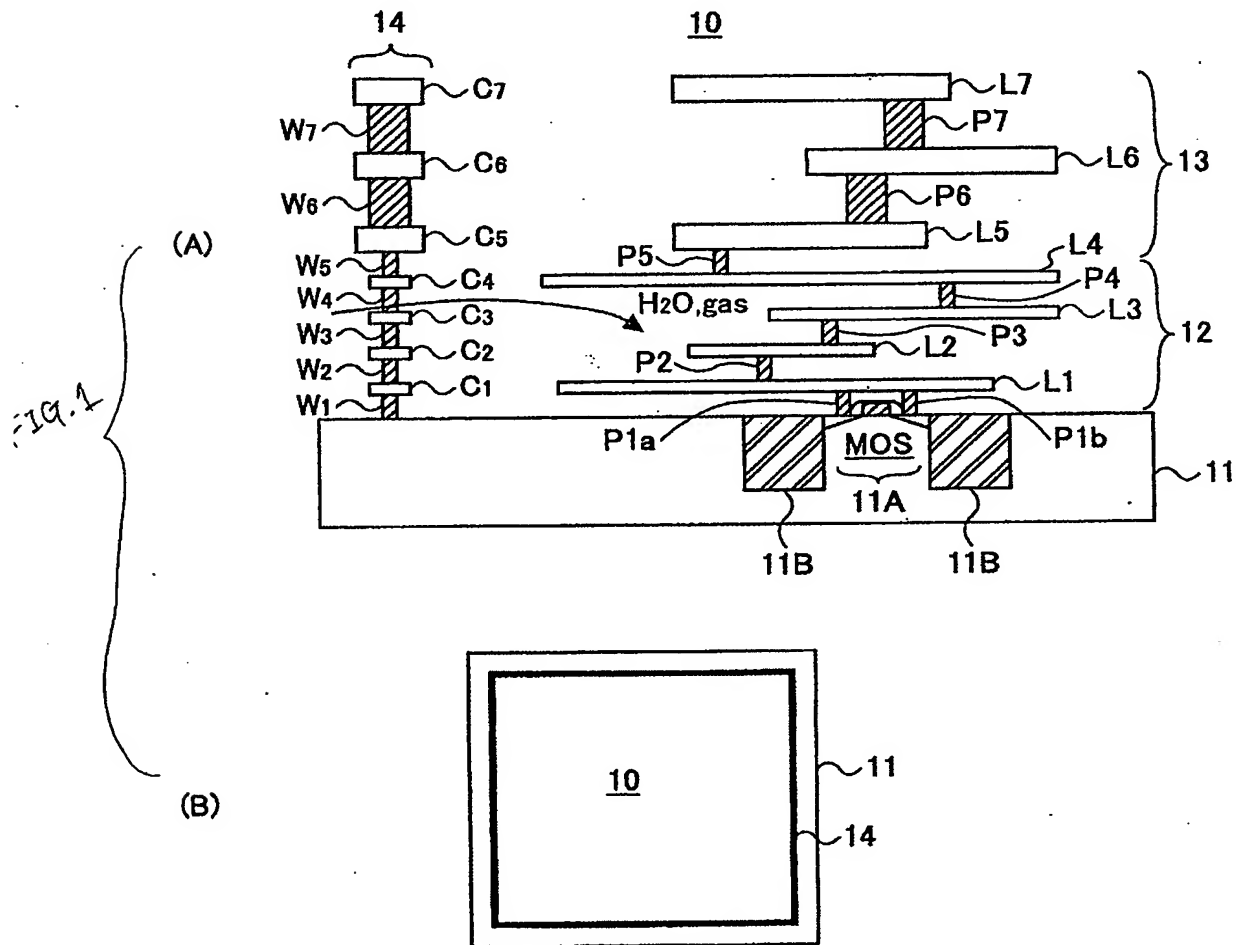
[Selected Figure] FIG. 9

整理番号=0241579

【書類名】 図面 [NAME OF DOCUMENT] DRAWINGS

【図1】 FIG.1 Diagrams showing the construction of a semiconductor integrated circuit having a conventional multilayer interconnection structure and a guard ring.

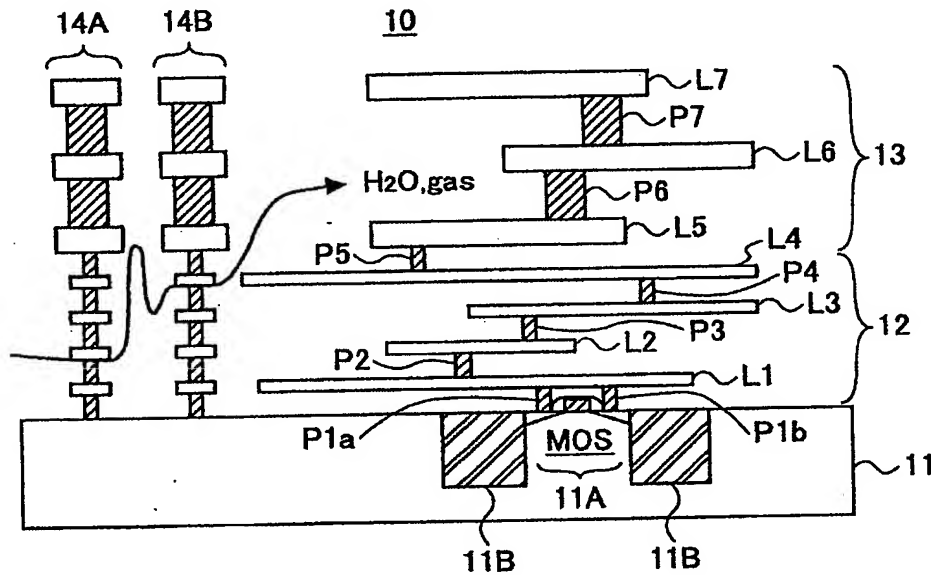
従来の多層配線構造と耐湿リングを有する
半導体集積回路装置の構成を示す図



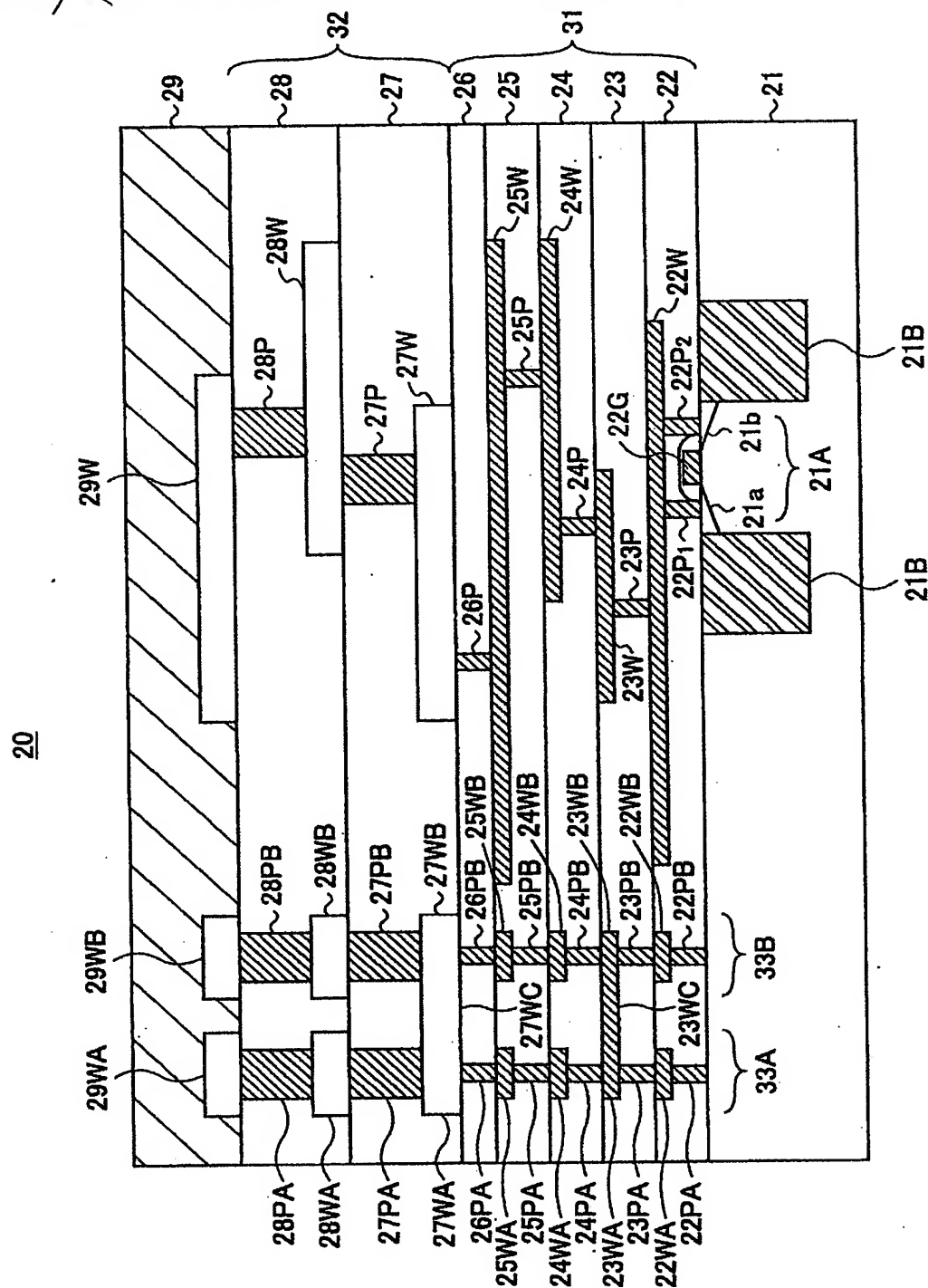
整理番号=0241579

~~【図2】~~ FIG. 2 Diagram showing the construction of a semiconductor integrated circuit having a dual guard ring structure and further the problems caused in such a semiconductor integrated circuit.

二重化耐湿リング構造を有する半導体集積回路装置の構成、およびかかる半導体集積回路装置において生じる問題点を説明する図

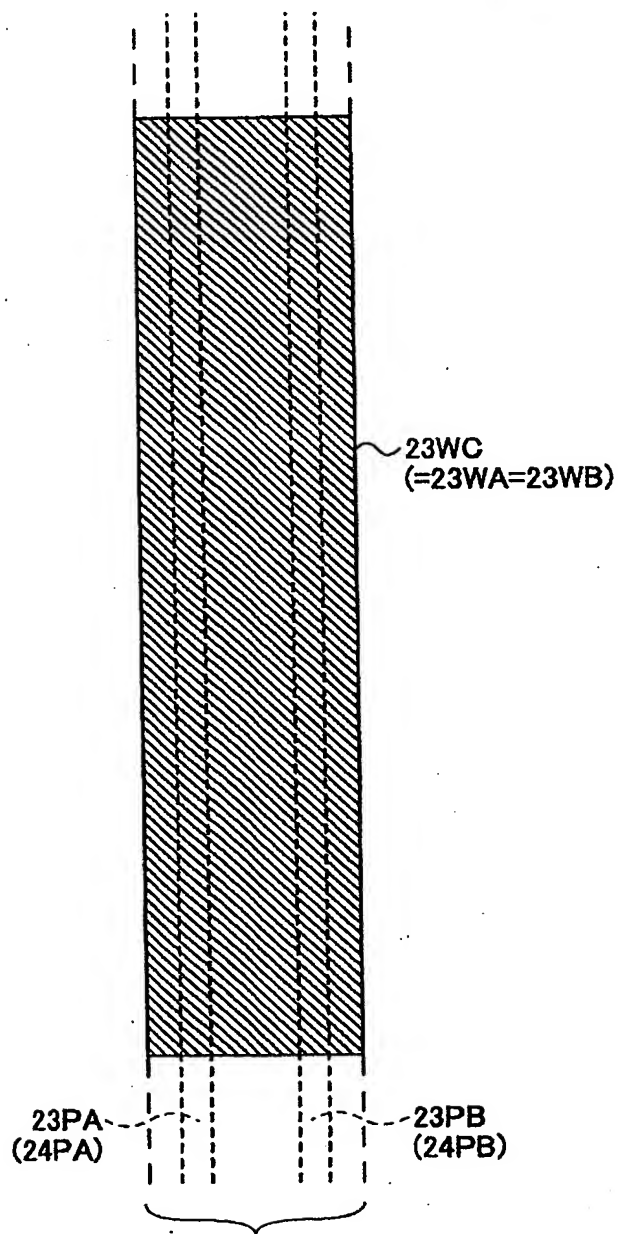


本発明の第 1 実施例による半導体集積回路装置の構成を示す図



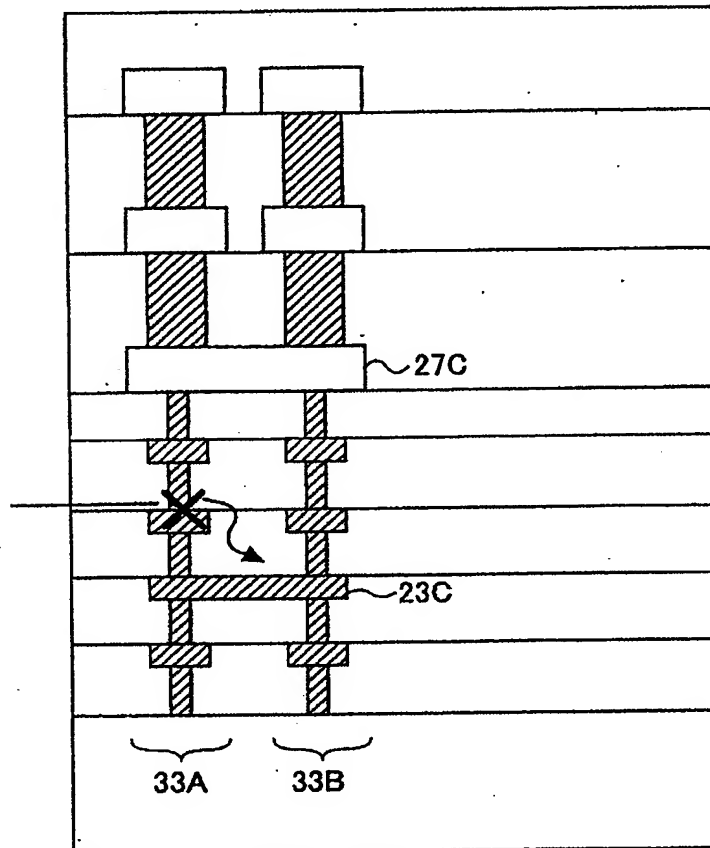
【図4】 FIG. 4

図3の一部を拡大して示す平面図 *Plan view showing a part of Fig. 3 with an enlarged scale.*



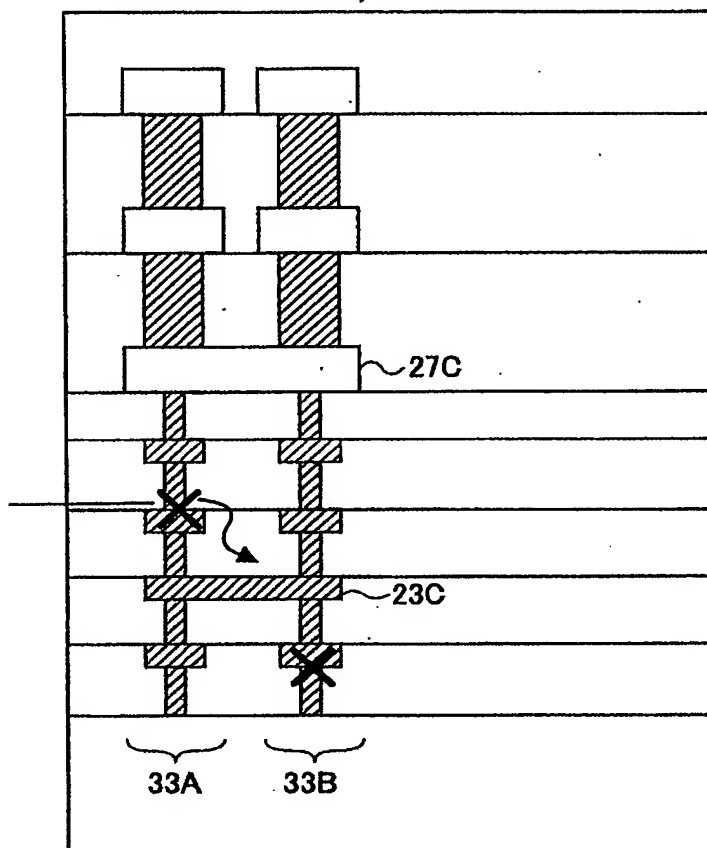
【図5】 FIG.5 Diagram explaining the function of the guard ring in the semiconductor integrated circuit of FIG.3.

図3の半導体集積回路装置における耐湿リングの作用を説明する図



【図6】 FIG. 6 Another diagram explaining the function of the guard ring in the semiconductor integrated circuit of FIG. 3.

図3の半導体集積回路装置における耐湿リングの作用を説明する別の図



【図7】 FIG. 7 Diagrams explaining the fabrication process of the guard ring used in the semiconductor integrated circuit of FIG. 3.

(A)~(C)は、図3の半導体集積回路装置における耐湿リングの製造工程を説明する図

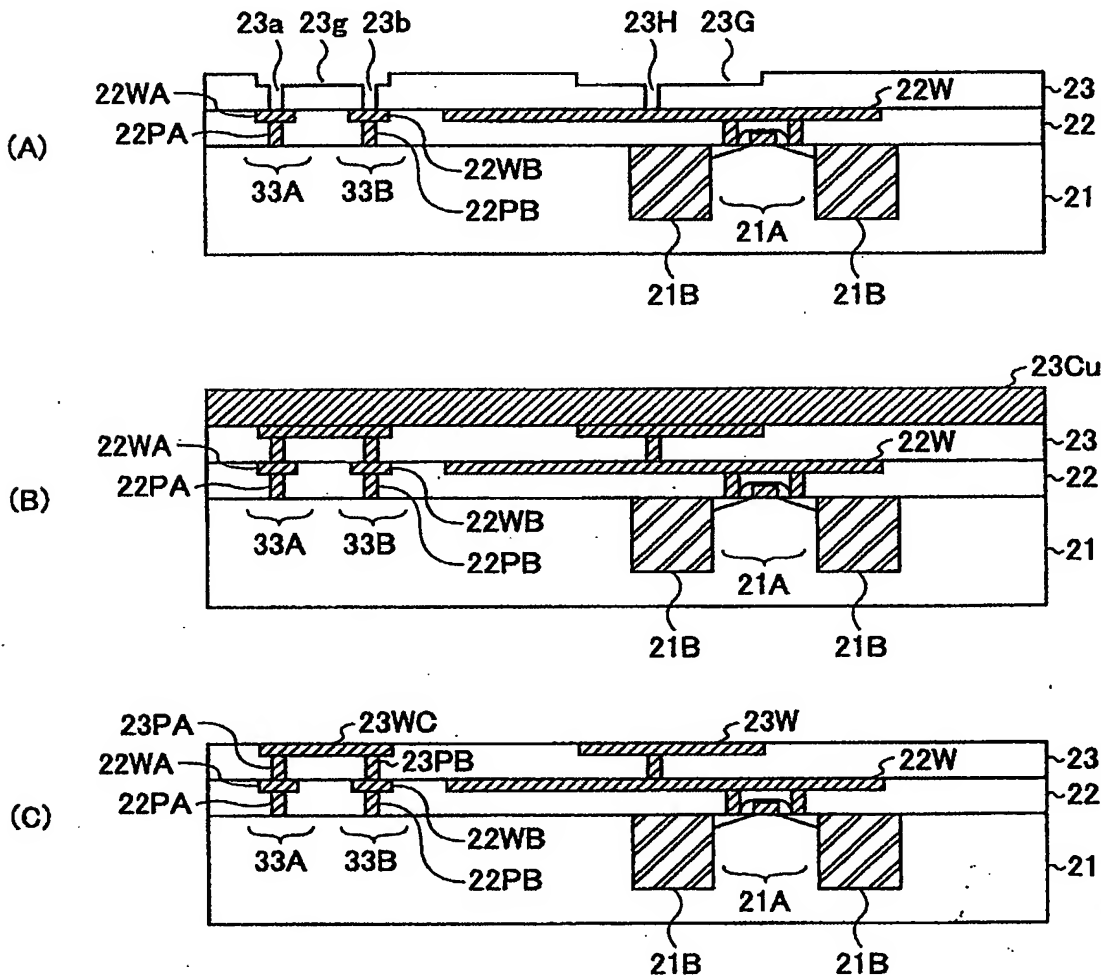
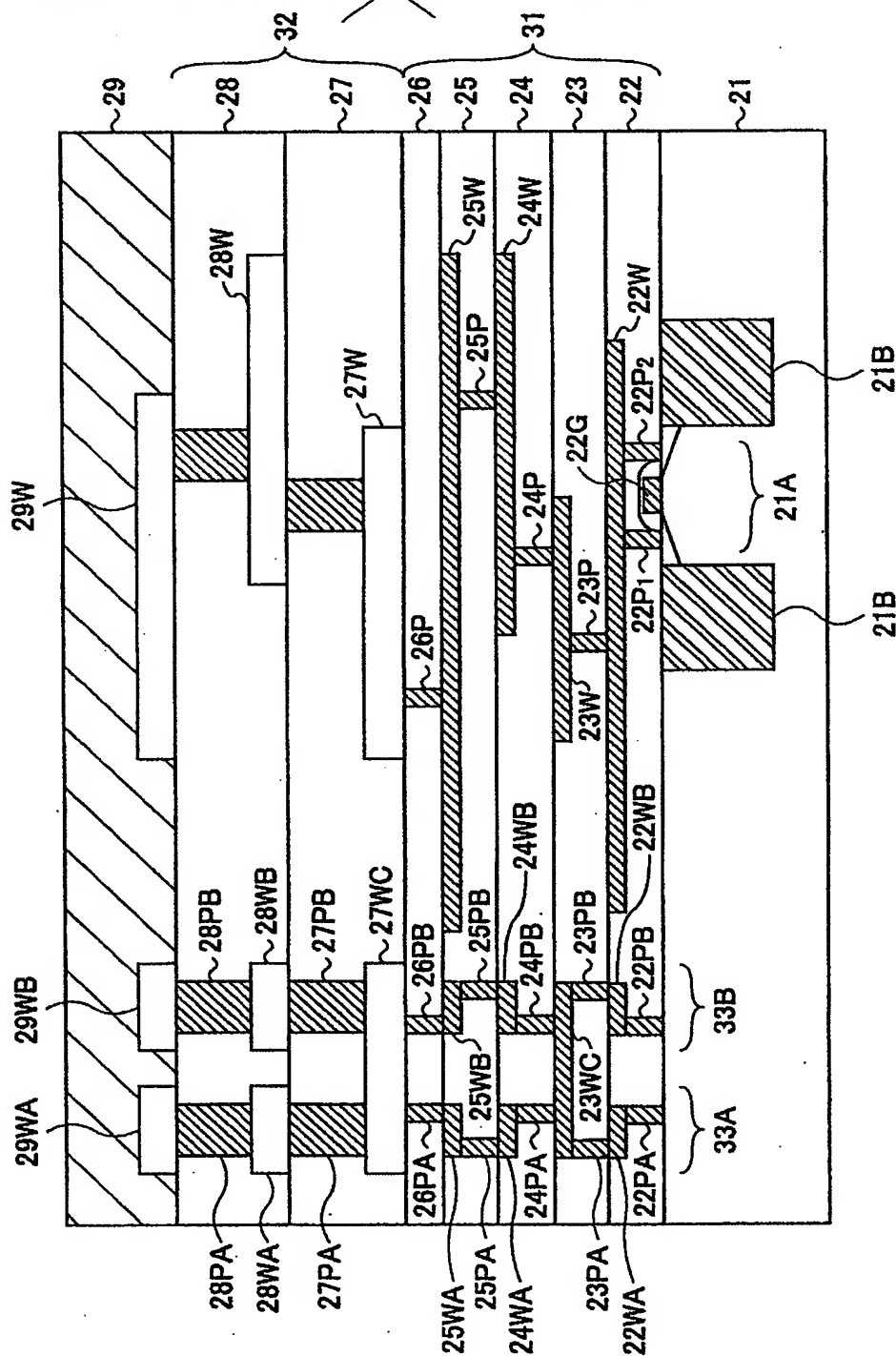
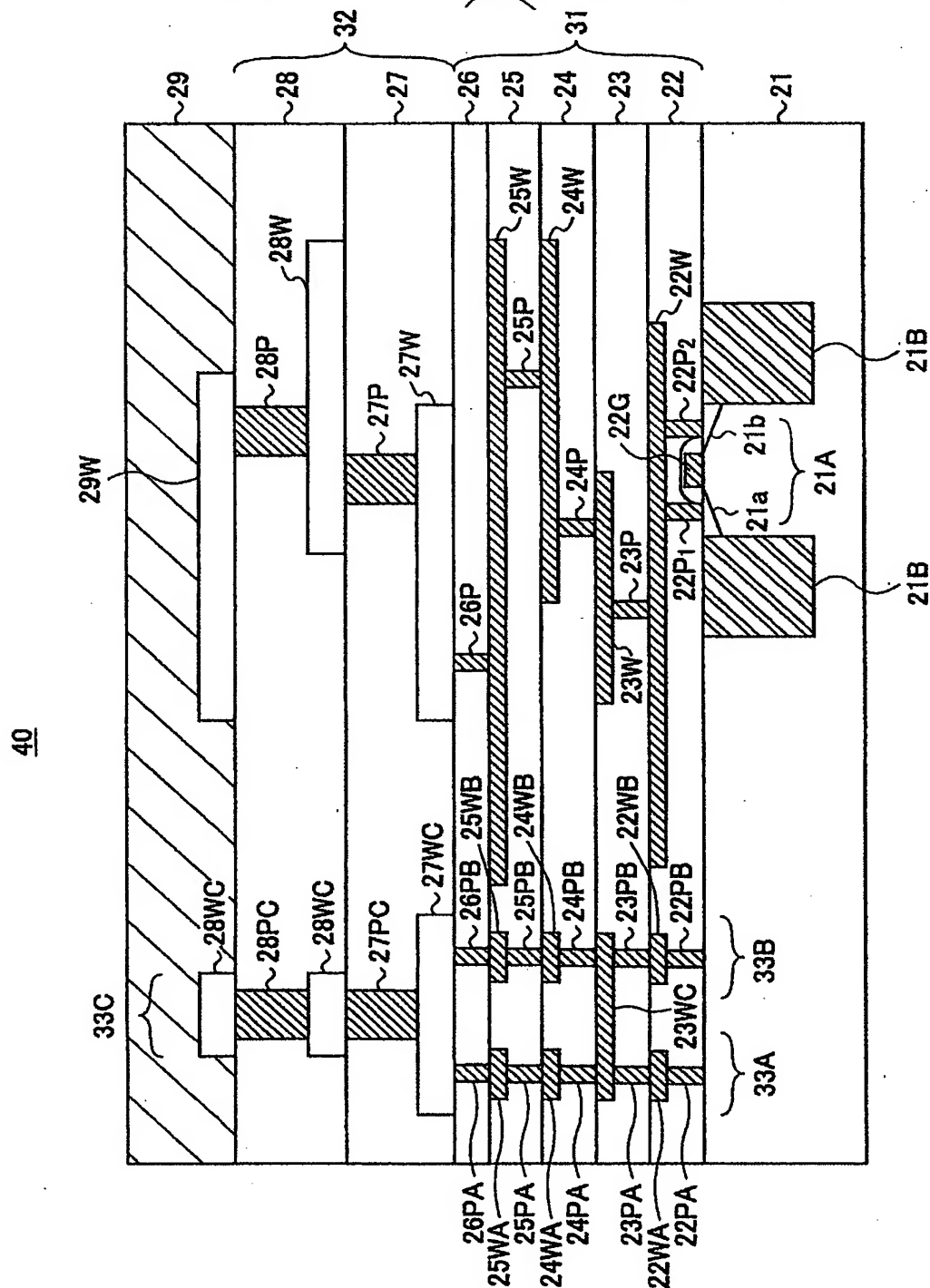


Diagram showing a modification of the semiconductor integrated circuit of FIG. 3.

図3の半導体集積回路装置の一変形例を示す図



本発明の第2実施例による半導体集積回路装置の構成を示す図



【図10】 FIG. 10 Diagram showing a modification of the semiconductor integrated circuit of FIG. 9.

図9の半導体集積回路装置の一変形例を示す図

